that various other changes and modifications may be made by one skilled in the art without departing from the scope of the invention.

What is claimed is:

1. A method of fabricating a field-effect transistor (FET) device, comprising the steps of:

forming nanowires and pads in a silicon-on-insulator (SOI) layer over a buried oxide (BOX) layer, wherein the nanowires are connected to the pads in a ladder-like configuration, and wherein the nanowires are suspended over the BOX;

depositing a hydrogen silsesquioxane (HSQ) layer that surrounds the nanowires;

cross-linking one or more portions of the HSQ layer that surround the nanowires, wherein the cross-linking causes the one or more portions of the HSQ layer to shrink thereby inducing strain in the nanowires, wherein the strain induced in the nanowires comprises a) tensile strain being induced in one or more portions of the nanowires and b) compressive strain being introduced in one or more other portions of the nanowires; and

forming one or more gates surrounding portions of each of the nanowires, wherein the gates retain the strain induced in the nanowires by the cross-linking step, and wherein the portions of the nanowires surrounded by the gates comprise channel regions of the device and portions of the nanowires extending out from the gates and the pads comprise source and drain regions of the device.

2. The method of claim **1**, further comprising the steps of:

removing one or more uncross-linked portions of the HSQ layer;

depositing a filler material to replace the one or more uncross-linked portions of the HSQ layer that are removed;

removing the one or more portions of the HSQ layer that are cross-linked using an etchant forming trenches in the filler material, wherein portions of the nanowires are exposed within the trenches;

forming a gate dielectric surrounding the portions of the nanowires exposed within the trenches; and

filling the trenches with a gate conductor to form the one or more gates of the device.

3. The method of claim **2**, wherein the one or more uncross-linked portions of the HSQ layer are removed using a developer selected from the group consisting of a Tetramethyl-ammonium hydroxide based developer and an aqueous mixture of sodium hydroxide alkali and sodium chloride salt.

4. The method of claim **2**, wherein the one or more portions of the HSQ layer that are cross-linked are removed using DHF.

5. The method of claim **2**, wherein the filler material i) can retain the strain induced in the nanowires by the cross-linking step, and ii) has an etching resistance to the etchant used to remove the one or more portions of the HSQ layer that are cross-linked.

6. The method of claim **2**, further comprising the step of:

forming an epitaxial SiGe film on regions of the nanowires exposed by removal of the one or more uncross-linked portions of the HSQ layer prior to deposition of the filler material.

7. The method of claim **2**, wherein the one or more portions of the HSQ layer that are cross-linked comprise dummy gates, the method further comprising the step of:

forming spacers adjacent to sidewalls of the dummy gates.

8. The method of claim **2**, wherein the gate dielectric comprises silicon dioxide (SiO_2), silicon oxynitride (SiON) or hafnium oxide (HfO_2).

9. The method of claim **2**, wherein the gate conductor comprises polysilicon, a metal or a combination of metals.

10. The method of claim **1**, further comprising the steps of:

removing one or more uncross-linked portions of the HSQ layer forming trenches between the one or more portions of the HSQ layer that are cross-linked, wherein portions of the nanowires are exposed within the trenches;

forming a gate dielectric surrounding the portions of the nanowires exposed within the trenches; and

filling the trenches with a gate conductor to form the one or more gates of the device.

11. The method of claim **10**, wherein the one or more uncross-linked portions of the HSQ layer are removed using a developer selected from the group consisting of a Tetramethyl-ammonium hydroxide based developer and an aqueous mixture of sodium hydroxide alkali and sodium chloride salt.

12. The method of claim **10**, further comprising the step of:

forming spacers adjacent to sidewalls of the gates.

13. The method of claim **10**, wherein the gate dielectric comprises silicon dioxide (SiO_2), silicon oxynitride (SiON) or hafnium oxide (HfO_2).

14. The method of claim **10**, wherein the gate conductor comprises polysilicon, a metal or a combination of metals.

15. The method of claim **1**, further comprising the step of:

forming contacts to the source and drain regions of the device.

16. The method of claim **1**, wherein the HSQ layer is deposited using spin-coating.

17. The method of claim **1**, wherein the one or more portions of the HSQ layer are cross-linked by exposure to e-beam or extreme ultraviolet (EUV) radiation with wavelengths shorter than 157 nanometers.

18. The method of claim **1**, wherein the cross-linking causes the one or more portions of the HSQ layer to decrease in volume by from about 5% to about 10%.

19. The method of claim **1**, further comprising the step of:

thickening the source and drain regions by epitaxy.

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